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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
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**Complete if Known**

Application Number	09/616,385
Filing Date	07/14/2000
First Named Inventor	Enric Musoll
Art Unit	2183
Examiner Name	Eric Coleman
Attorney Docket Number	P3809

Sheet 1 of 5

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
EC		US- 5600837 A *	02-04-1997	Artieri, Alain	
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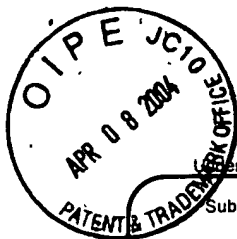
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Examiner Signature		Date Considered	6/27/03
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Signature

*Eric Coleman*

Date  
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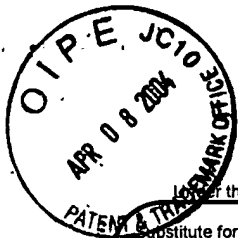
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		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
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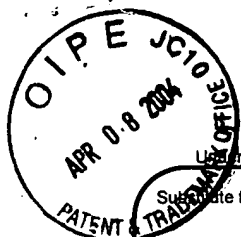
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		* The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
		* MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
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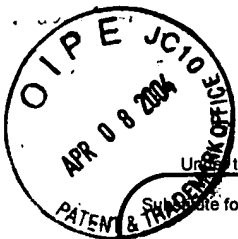
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		* DONALSON ET AL., "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance", 26th Hawaii Conference on Systems Sciences, 1993, pp 448-456, vol. 1	
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		* BRADFORD, JEFFREY et al., Efficient Synchronization for Multithreaded Processors, Workshop on Multithreaded Execution, Architecture and Compilation, January-February 1998, pp. 1-4	

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